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PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Binary Information Stores

We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Company incorporated under the laws of the State of New York, in United States of America, of Armonk, New York 10504, United States of America, (assignees of HANS P. SCHLAEPPI), do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to binary information stores, and aims at providing such a store in which an initial driving pulse gives, or can give, rise to reflected pulses which are delayed in time so that they can be differentiated from the initial pulses without the use of sophisticated apparatus.

Pulses reflected from the ends of the drive lines remote from the input lines, can be used to switch the magnetisation of the elements to the hard direction, for subsequent regeneration cycles, when the elements are provided as films of uniaxial anisotropic magnetic material.

One kind of magnetic film memory for the storage of digital information comprises a three dimensional array of memory cells having the property of uniaxial magnetic anisotropy, with pulse sources and control circuits, each associated with one plane of the memory, for the switching of the memory cells to the direction of hard magnetization, and a plurality of read lines each associated with one row of the memory cells and in which a voltage is induced when the cells are magnetized in the direction of hard magnetization. The present invention may advantageously be embodied in such memories.

In such memories, the control circuits are designed as pulse switches and/or pulse accumulators. A pulse switch has an input formed of a single distribution line on which a pulse generated by any source is carried; in addition, it further comprises several output lines which are connected at suitably selected points to a distribution line *via* a non-linear circuit component ("switch") in such a manner that closing of a single "switch" causes the pulse on the distribution line to be supplied, more or less completely, to the output line associated with the closed switch. On the other hand, a pulse accumulator is provided with several input lines but only one output line in the form of a collector line; the input lines are connected to the collector line at suitable points thereof, either directly or via individual switches, so that a pulse passed to the collector line by one of the input lines will continue, entirely or partly, on this collector line. In explanation of the invention, the application of pulse switches and accumulators and the problems arising in connection therewith are discussed in conjunction with a word-organized magnetic film memory operating according to the orthogonal access method.

Such a memory may employ thin magnetic films as memory cells which possess the property of uniaxial anisotropy. Such films have so-called "hard" and "easy" directions of magnetization which are in the plane of the film at least substantially perpendicular to one another. The behaviour of these memory cells is determined by the various positions the magnetization vector can assume.

The magnetization vector or a magnetic film memory cell with uniaxial magnetic anisotropy may assume, in the so-called "easy" direction of magnetization, either of two equal positions which may be associated with the binary digits "1" and "0". If such a memory is magnetized, by a so-called driving field, in the hard direction, i.e. in the direction perpendicular to the easy direction, the magnetization vector will switch to the hard direction. If the "driving field" is removed, the magnetization vector will return to one of the two possible stable positions in the easy direction.

[*Price* 4*s.* 6*d.*]

If a current is maintained in a write line perpendicular to the line causing the magnetization into the hard direction, the magnetization vector will adjust to that one of the two possible positions in the easy direction corresponding to the polarity of the field operative on the cell through the writing line. If a driving field is again applied in the hard direction, a voltage is induced in the read line parallel with the write line by the change of direction of the magnetization vector, the polarity of said voltage being dependent on the previous position of the magnetization vector in the easy, i.e. stable direction.

The binary information which was previously supplied by the write line and which was stored by the position of the magnetization vector in one of the two stable positions, may therefore be taken from the read line.

In magnetic film memories the individual memory cells are arranged three-dimensionally. In this three-dimensional arrangement, the word lines generating the driving field for the temporary magnetization of the cells when writing or reading the information, run along vertical columns of elements. Running horizontally in the three-dimensional arrangement are the so-called write lines and read lines through which the binary information to be stored is either supplied or obtained. For example, in a read operation current is passed through a single word line, which current causes all of the magnetic film cells of the associated vertical column to switch into the hard direction of magnetization. Thereby, in all of the read lines passing the corresponding cells, a voltage is induced by the change of position of the relative magnetization vectors the polarity of which depends on the binary information stored in each cell. The information of the word composed of several bits thus will appear in the said associated read lines almost at the same time.

In order to ensure that only one word line is energized at a time, i.e. that only the memory cells of one column are magnetized in the hard direction, these word lines are subdivided into groups. All of the word lines associated with a certain group are connected to a distribution bus common to the group by means of a non-linear switching member; the distribution bus may be supplied with a driving pulse by a pulse generator associated therewith, and as many pulse generators and distribution busses must be provided as there are groups of word lines.

In the memory disclosed as an embodiment of the present invention, each switch is composed of a diode by which the associated word line is connected to the distribution bus of its group. The other ends of the word lines are connected to collector lines. Each of the collector lines may be grounded by means of an electronic switch. Connected to each of the collector lines is a word line of each group. Appropriate selection of the potentials of the line systems enables all diodes to be blocked when the switches are open and a driving pulse passing through a distribution bus to reach only one diode without blocking bias, i.e. the one of which the associated word line is connected to both the distribution bus supplied and the collector line now grounded. It can readily be seen that the driving pulse is passed into the associated word line by this diode.

Magnetic film memories of the type described operate satisfactorily as long as the read and write speeds are such as to make the delays in the word, write and collector lines and the distribution busses short or comparable with the signal rise times. However, the present electronic computing and data processing machines require memories which do not meet this condition and in which the finite velocity of propagation of the pulses in the various lines must be taken into account.

For each volume of a three-dimensional memory arrangement, there is a lower limit of the signal rise times and, accordingly, of the access time below which operation is disturbed by the reflections generating on the lines. In the memory arrangement selected as an example, the following effects are *inter alia* observed which may give rise to such disturbances:

a) At the connection point adjacent to the conducting diode, the energy of the driving pulse is divided into three portions: the useful word pulse which passes *via* the word line to the storage elements, and two disturbing pulses one of which continues to run on the distribution bus while the other returns to the generator. At the ends of the distribution bus, the energy of the disturbing pulses is partly absorbed, but a considerable portion of their energy is reflected there and appears, after the respective propagation time at the point of connection, as a delayed contribution to the original word pulse. In the event the delay is small compared to the rise time of the driving pulse, these effects are observed only as a capacitive load on the generator. In fast memories, however, this does not apply; the various delayed contributions add as many discrete steps to the word impulse, whereby the time-position with respect to the original word pulse depends on the propagation time of the disturbing parts. This makes the wave form of the word impulse dependent on the position of the connection point on the distribution bus so that in each word line a particular word pulse form different from the others become operative. This causes, part from a delay in the read and write processes, read signals to appear differing from one word to the next, which may mean extraordinary requirements for the read amplifiers.

b) A word pulse on a collector line not only meets the impedance of the collector line at

the connection point of the word line, but, in parallel therewith, the impedance of all other word lines connected to this collector line. The very low termination impedance of the word line thus obtained results in an almost complete reflection of the word pulse at this point of connection, which in turn results in a current step in the effective word pulse of almost 100% of the original word driving current which current step is delayed relative to the latter by a propagation interval different for each bit of information. The effective word pulse form and, accordingly, the read signal will therefore be different from one bit to the other.

c) The resistance of the electronic switches connecting the collector lines to ground being much greater than the total impedance of the collector line also in the closed condition, the word pulse generates residual voltages on the collector line which propagate as disturbing pulses into all inactive word lines of this collector line; these disturbing pulse therefore cause as many memory cells on each read line to switch out of their home position, which may result in a plurality of disturbing signals which, while small, will add up on the read line and reduce the signal/disturbance ratio or cause misinterpretation of the useful part of the read signal by the read amplifiers.

It is an object of the present invention to enable the design of particularly fast memories by elimination of adverse effects of certain reflection and propagation effects.

More particularly, the present invention is intended to eliminate, in fast-operating memories employing distribution busses and/or collector lines of the type mentioned above, the limitation of the obtainable read and write times by certain delay effects without creating other speed-limiting effects by the measures taken.

In certain memory configurations employing the present invention, the collector lines are omitted, so that only distribution busses are present. The nature of the memory cell employed and its mode of operation are not essential for the understanding of the invention.

The memories according to the present invention are characterized by the fact that additional line lengths are arranged in the distribution line system and that further line lengths are connected in series to the inputs of the collector lines, if used, which bring about the desired increase of the propagation time of the disturbing pulses. This enables the energy which may be reflected at the ends of the distribution busses and/or connection points of the collector lines to be delayed to such a degree that it will reach the word lines only after the read or write process is effectively terminated, so that these processes cannot be detrimentally affected by the reflected energy.

The present invention is illustrated by way of example in the accompanying drawings, in which:—

Fig. 1 is a schematic view of a magnetic film store;

Fig. 2 shows the wiring diagram of a distribution bus, for the store shown in Fig. 1, and

Fig. 3 is a diagrammatic view of a second embodiment of the invention.

In the magnetic film memory according to Fig. 1 four plates 10, 20, 30 and 40, are provided which are placed behind one another and which carry the individual magnetic film memory cells. It is assumed that each plate is provided with four vertical columns each having five individual memory cells so that each plate carries a total of 20 cells. The memory cells, which are thin magnetic films vapour deposited on the plates, have uniaxial magnetic anisotropy, the direction of the easy magnetization being vertical and that of the hard magnetization horizontal.

Passing in front of the individual magnetic film cells of each column on each plate in the vertical direction are the word lines. The word lines associated with plate 10 are designated 12, 13, 14 and 15, those associated with the second plate are designated 22, 23, 24 and 25, etc.

Each word line has its upper end connected to a diode 12*a*, 13*a*, 14*a* or 15*a*. The word lines associated with each plate are connected, *via* their associated diodes, to a respective distribution bus 16, 26, 36 or 46. Each of the said distribution busses is fed by a pulse generator 17, 27, 37 or 47, respectively. The pulses are returned *via* ground as indicated at 18, 28, 38 and 48. The lower ends of the word lines are connected to collector lines 60, 61, 62 and 63 in such a manner that any one word line (15, 25, 35 and 45) associated with each distribution bus is connected to a particular collector line (e.g. 63). The lower ends of the word lines, unless completely drawn, are only indicated. Each collector line 60 through 63 may be connected to ground when a normally open switch 60*a*, 61*a*, 62*a* or 63*a* is closed. In order to show that the switches present a finite resistance when closed, they are represented by a series connection of a switch with a resistor.

In order to ensure permanent-blocking of the diodes 12*a* to 45*a* during the passage of the driving pulses, the circuitry formed by one collector line and the connected word lines, is at a bias potential which is higher than the temporary potential of any distribution bus occuring at the peak value of the drive pulse. This is schematically indicated in Fig. 1 by the voltage source 100 connected to the collector lines *via* resistors 80 to 83. If one of the switches 60*a* to 63*a* is closed, the associated circuitry is connected to ground potential so that one diode in each distribution line remains without blocking voltage.

If one of the pulse generators 17, 27, 37 and 47 is switched on after one of the switches 60*a* to 63*a* has been closed, the driving pulse passing through the associated distribution bus will arrive at the one diode without blocking voltage; accordingly, it will continue its way, *via* this diode, into the connected word line. If pulse generator 27 for example supplies a pulse while at the same time switch 63*a* is closed, a current will pass from pulse generator 27 through distribution bus 26, diode 25*a*, word line 25, collector line 63, and switch 63*a*. Diode 25*a* is thus the only diode which is energized and not blocked. This causes magnetic film memory cells 225 of the right-hand column on plate 20 to be magnetized in the hard direction. Arranged transversely to the word lines, i.e. horizontally in the drawing, are read lines 70. The upper horizontal row of magnetic film memory cells on plate 10 is traversed by read line 70*a*, the second row by the read line 70*b*, etc. In order to explain the function of the read lines it is assumed that the magnetic film memory cells of column 113 on plate 10 contain information as indicated by the magnetization vectors located in the easy direction of magnetization. It may be assumed here that the digit "1" corresponds to an upwardly directed magnetization vector, and the digit "0" to one downwardly directed. The information registered in the first four cells of the said column thus corresponds to the information "1", "1", "0", "1". If pulse generator 17 is caused to supply a pulse to sense this information while switch 61*a* is closed, all cells are magnetized in the hard direction, the magnetization vectors of the cells 113a, 113*b* and 113*d* rotating in the clockwise direction, and that of cell 113*c* in the counterclockwise direction.

This causes a positive pulse corresponding to the digit "1" to be passed through read lines 70*a*, 70*b* and 70*c*, while a negative pulse corresponding to the digit "0" appears in the read line 70*c*. The information stored has thus been emitted by read lines 70. The storage of information in the memory is effected in the manner characteristic of the so-called perpendicular operating process of magnetic memories: arranged parallel with, and above the read lines 70 are write lines, not shown in Fig. 1 for the sake of clarity. For write-in, current is passed through these write lines in a direction which corresponds to the information to be stored. To write a particular word, the associated switch 60*a* to 63*a* is closed, and the associated pulse generator (17, 27, 37, 47) is energized during the presence of this writing current. The writing current is maintained until the word pulse has virtually faded so that the direction of rotation of the magnetization vector is controlled by the writing current in the write line as it returns to the easy direction.

The drive pulses supplied by pulse generators 17, 27, 37 or 47 and the word pulses derived therefrom are divided and reflected at the unavoidable connection points in the circuitry: if the pulse propagation time becomes greater than the pulse rise time, i.e. when the memory is operating at high speed, the wave-form of the effective word pulse is influenced to an extent which differs from word to word, and this may have adverse effects. In order to explain this, reference is made to Fig. 2 which shows, by way of example, distribution bus 16 with pulse generator 17. The same reference numerals are used as in Fig. 1. If it is assumed that diode 14*a* is conductive at a certain instant, the current supplied by pulse generator 17 is divided a first portion I_{11} passing through word line 14, a second portion I_2 continuing on distribution bus 16, and a third portion I_3 being reflected and returning to the pulse generator.

Since an ideal termination of both ends of the very low-resistance distribution busses cannot be achieved and often is undesirable for reasons of energy consumption, current I_2 is at least partially reflected at the right-hand end of the distribution bus and returns to the point of connection as current I_2^1, and current I_3 is also partially reflected at the output terminal of pulse generator 17 and returns to the point of connection of the conducting diode as I_3^1. Reaching that point, the original drive pulse and the reflected portions delayed by their propagation times combine into a three-step drive pulse operative at diode 14*a*: the amplitudes of these steps depend on the impedance conditions on the lines and their terminations, while the times of appearance of the steps depend on the propagation times of the reflected parts of the pulses which in turn are a fuction of the position of the conductive diode on the distribution bus. Accordingly, the effective drive-pulse form is different for all the word lines connected to one and the same distribution bus. If the rise times of the drive pulses supplied by the pulse generator become comparable to the propagation times described, these steps are more or less blurred, and an effective rise time of the word pulses appears after the steps have been evened out. This effective rise time may then be considerably shorter than the original rise time of the drive pulses and it will differ from one word line to the next. Depending on the rise time of the word pulses, however, is the read voltage appearing on the read line so that one and the same read amplifier would have to process signal pulses of different amplitude and duration, which leads to increased errors. This difficulty might be overcome by integration in the read amplifier but this would reduce the operation speed of the memory. The stepping of the word pulses causes them to become longer, which further contributes to a reduction of the operation speed.

In order to avoid these disadvantages, the distribution bus could at either end be terminated with its characteristic resistance. This however, would entail the serious disadvantage that a loss of output energy of almost 50% would have to be accepted owing to the in general relatively high-resistance output impedance of the pulse generators. In addition, accurate matching is difficult to obtain in practice in view of the very low-resistance lines.

In the present example a length of line 16*a* having the same characteristic impedance as the distribution bus is inserted between the inlet of distribution bus 16 and the outlet of pulse generator 17. An equal length of line 16*b* is connected to the end of the distribution bus remote from the generator, and this length is terminated by resistor R corresponding to the characteristic resistance of the distribution bus. The length of the two lines should be such as to ensure that the read operation is effectively completed when the reflections reach the word line.

The reflections occurring owing to the absence or imperfection of correct termination can, however, under the teaching of this invention, also be employed favorably to influence the effective word pulse form if the circuit parameters are suitably selected.

In the magnetic film memory discussed here, the reflected pulses returning from the two ends of the distribution bus may be employed, for example, to turn off the word pulse prior to the decay of the primary drive pulse. To this end, the reflected pulses must reach the conductive diode with a polarity opposite to that of the original drive pulse, since, owing to the non-linear characteristic of the diode, a relatively small reduction of the amplitude of the drive pulse by the negative contribution of a reflected pulse, will cause a considerable reduction of the diode current and, along with it, of the word pulse amplitude.

This condition is automatically met regarding the portion I_3 of the drive current returning to pulse generator 17 since the connection point of the conductive diode always represents an under-match for the drive current so that the latter and I_3 have different polarity; in addition, the output of the pulse generator in practice always represents a resistance compared to the distribution bus so that the reflection of I_3 at 17 occurs without reversal of polarity. Accordingly, when I_3^1 returns to the diode, it possesses opposite polarity relative to the drive pulse.

As regards the reflected portion I_2^1 of the continuing drive pulse portion I_2, the condition of the sign reversal can be met by undermatching in the termination: $R<Z_o$, where Z_o is the characteristic impedance of bus 16.

The said reduction of diode current I_1 after the appearances of the reflected pulses causes both, the remaining drive pulse current portion and teh currents I_2^1 and I_3^1 to be directed away from the word line into the distribution bus. This results in secondary reflections I_2^{11} and I_3^{11} which reach the connection point delayed by a further propagation time relative to I_2^1 and I_3^1. The portion I_2^{11} formed by reflection of the containing current I_2^1 at the substantially open output of 17 undergoes no change of sign so that I_2^{11} tends to continue blocking the diode. On the other hand, portion I_2^{111} of I_2^{11} again reflected at termination R is of equal polarity owing to $R<Z_o$ as the original drive pulse and could accordingly again partly open the diode if it were of sufficient amplitude, which would be undesirable. With the postulation that I_2^{111} may have only 10% of the drive current amplitude in order to eliminate this possibility, and with all energy losses apart from those involved in termination R disregarded, the following dimensioning condition for R results:

$$R=0.7\ Z_o \pm 40\%$$

The portion I_3^{11} also tends to again open the diode; I_3^{11} is, however, necessarily smaller than I_2^{11} coincidentally with which it reaches the diode, so that I_3^{11} can not open the diode.

This shows how the drive pulse reflections occurring at the connection points of the distribution bus can be rendered innocuous. Against this, it must be accepted that the access time of the memory is increased by the propagation time in the extended line length. Since only times of the magnitude of one half of the rise time of the read amplifier are involved, which virtually amount to only a small fraction of the access time, this loss of time is generally acceptable.

Also the reflections necessarily encountered in the word lines can be timed so as to prevented from adversely affecting the read operation.

The following explanations refer to Fig. 1. As previously stated a word pulse passing *via* a word line (e.g. 12) to the collector line (e.g. 60) meets an impedance which is very low relative to the characteristic impedance of the word line. This impedance is composed of the parallel connection of all other word lines connected to this collector line (here: 22, 32, 42) and the internal resistance of the closed switch (here 60*a*). Owing to this short-circuit at the end of the word line, which is almost perfect in practical memory arrangements, the word pulse is reflected into the word line with reversed sign, which causes the current on the word line to rise to almost double its value. Owing to the reflection, the word pulse fades in steps. The permutation of the steps and the resulting form of the effective word pulse are different from bit to bit.

This effect affects the form of the signal sensed, which renders circuit measures necessary (such as the previously mentioned integration of the read signal in the read amplifier)

which have the effect of slowing down the memory cycle. Furthermore, the composition of the word pulse of temporally permutated steps due to the reflection, results in an extension of various phases in the memory cycle.

The elimination of the adverse effects of the reflections by separation of the pulses in time from their interfering reflections is advantageously achieved through extensions of the word line between the memory matrix and the collector lines by a suitable length (Fig. 1).

A further adverse effect occurs because it is virtually impossible to shirt-circuit the collector lines to ground by means of switches 60*a* to 62*a*. The residual impedance of a closed switch will always be larger than the very low impedance of the collector line formed by parallel connection of all non-selected word lines connected to a collector line. (The selected word line is the line carrying the word pulse.) Accordingly, the word pulse divides when it meets the collector line in the proportion of the word-line impedance to collector-line impedance, and that portion of the pulse which enters the collector line enters into all word lines connected but not selected. This causes the magnetization vectors of all of the non-selected memory cells to be deflected from their stable position so that each cell will induce a signal in its respective read line. While these interference signals are individually small, they can add up on the read lines so that reading errors may occur when the conditions in the memory are unfavorable. This effect is again eliminated by the extension of all the word lines by L (Fig. 1).

The additional length L of the word lines is determined by the propagation time T along the double length 2L. In order to avoid deterioration of the word pulse form, T must be greater than the word pulse duration. In order to eliminate disturbance of the read operation, T should be equal or greater than the interval beginning with the rise of the read signal and ending when the information read is passed on to the circuits following the read amplifier. Depending on the magnitude of the two disturbance effects, dimensioning will be made in accordance with the first or second condition or according to that one yielding the greater T.

Extension of the word lines is likely to avoid the said adverse consequences of reflections and imperfect switches without resulting in any retardation in the memory cycle. It should be noted that the loss in the additional length l of the word lines, which is unavoidable, is desirable since it causes the amplitude of the word pulse reflected with a delay to be reduced relatively to the original word pulse; if this amplitude ratio is sufficiently great, the write current must be interrupted not only after the fading of the reflected word pulse but immediately after the fading of the original word pulse, which also contributes to a shortening of the memory cycle.

In a practical embodiment of the invention, the following space-saving arrangement of the above additional line lengths has proved to be advantageous: The strip-like extensions of the word lines are applied to a first plastics sheet. A second plastics sheet covered by a closed, grounded metal film is placed underneath the first sheet and the whole "sandwiched" rolled up in the manner usual in the manufacture of paper condensers. Connection to the switches is taken laterally from the center of the roll.

In the example to be described with reference to Figure 3 the driving pulse on the word line which is reflected at the end remote from the pulse source is used to switch the magnetization of the memory cells to the hard direction for the subsequent regeneration cycle. Care must be taken, however, to ensure that after passing through the memory arrangement the reflected pulse is absorbed or at least attenuated sufficiently so that no reflection at the diode takes place which would impair the information stored. In the first embodiment shown in Figures 1 and 2, this is accomplished by the circuit itself. Owing to its reversa of polarity when reflection takes place, the pulse returning e.g. on word line 14, brings diode 14*a* into the conducting state and is in part absorbed in the diode impedance. The remainder of the pulse passes on to distribution bus 16. The resulting attenuation, however, is sufficient. To estimate the conditions arising in practice, let it be assumed that the series connection of word-line impedance W and effective diode impedance D is roughly equal to the impedance Z of the distribution bus. On that assumption, the impedances for the reflected pulse are matched at the diode when the impedance ratio is $W/D=3$. Half of the reflected word pulse propagates along the right and half along the left branch of distrition bus 16, toward pulse source 17 and terminal resistance R (cf. Fig. 2), respectively. On the above assumption that $D+W=Z$, the amplitude of this partial pulse comprises at most 25% of the original word pulse, i.e. is smaller than the amplitude of the reflected current pulses I_2 and I_3; thus partial pulses propagating along distribution bus 16 can be regarded as innocuous. If the impedance ratio varies between $W/D=1$ and $W/D=\infty$, i.e. the diode conducts infinitely well, then the reflection factor will vary from $+1/3$ to $-1/3$. The practical conditions in the first embodiment are thus always such that no major disturbing multiple reflections arise.

A necessary condition for the effectiveness of the doubly utilized driving pulse is nearly complete reflection at the end of the line remote from the pulse source. This is best achieved by a full short-circuit as the termination of the line. However, even the circuit in the first embodiment shows, at the termination

of the word lines, behaviour very similar to a short-circuit. In the second embodiment, the word lines of the magnetic film memory are terminated with a short-circuit. This circuit design necessitates a different access method for the individual word lines. Fig. 3 shows as an example a magnetic film memory in which access to a word line takes place *via* transistor switches 51 to 56 arranged in pyramid form. The memory plane 50 has four word lines 11, 21, 31, 41 passing across the magnetic film memory cells parallel to the easy direction e. The ends of the word lines nearer pulse source 57 are connected to the collector electrodes of output transistors 51 to 54 of the switch pyramid. Owing to the pyramid-like arrangement of transistors 51 to 56, the $2^2=4$ word lines are individually accessible to pulse source 57. The addressing of the word lines is effected by means of an address register 58, which is connected to the base electrodes of transistors 51 to 56 *via* control lines 64 to 67. The magnetic film memory cells are represented only schematically in the figure. The principle of information storage is the same as in the memory shown in Fig. 1. The end of each word line 11, 21, 31, 41 remote from pulse source 57 is grounded or at least terminated with a resistance which is considerably smaller than the characteristic impedance of the word line. To delay the pulses passing to and fro, a suitable pulse-delaying element 86, consisting e.g. of a portion of conductor line, is placed between each word line and the electric termination, e.g. the point of connection with ground potential. For the purpose of absorbing reflected pulses, word lines 11, 21, 31, 41 comprises, at their ends nearest transistors 51 to 54 suitable shunt means, e.g. a diode 84 connected in proper polarity. In many cases the resistance 85 is merely the internal resistance of diode 84 itself, so that in many practical embodiments there is no need for a separate resistance element 85. The resistance 85 is shown in Fig. 3 primarily in order to clarify the mode of action of the shunt means.

For the sake of clarity, only a few of the assumed 32 memory elements arranged in 4 words of 8 bits are drawn into the one memory plane 50 shown in Fig. 3. In this second embodiment the direction of easy magnetization designated with e is vertical; the resulting magnetization vector of each film element can assume one of two positions in the easy direction to which are assigned the binary digits "0" and "1". Sense lines 71 to 78 and write lines 91 to 98, which permit access to the bits of the word selected, run parallel to each other and orthogonally to the word lines, with which the individual words can be selected. For this reason the write lines in a word-organized magnetic memory are also termed bit lines. Each sense line 71 through 78 is connected to a sense amplifier 79, which is capable both of adequately amplifying the relatively weak voltage signals induced in the sense line when the magnetization of the memory cells of the word selected is switched from one of the two positions along the easy direction to the hard direction, and of delivering distinct output signals corresponding to the stored binary values. The sense signals, amplified to the voltage level of the signal of the computer, can be passed either to the computer *via* the output terminals of the sense amplifiers, e.g. information from sense line 78 *via* terminal 78*a*, or to a regeneration loop comprising a device 90 to be described later. Each write line 91 to 98 is provided with a write amplifier 99, which receives the binary values to be stored either *via* the regeneration loop or from the computer *via* its input terminal, e.g. 98*a*; and which is capable of delivering to the associated write line, e.g. 98 but pulses suitably polarized for the write-in process. As has already been mentioned, each pair of bit and sense lines is provided with a device 90 comprising delay means for the regeneration of the magnetic film memory. As the stored information is destroyed by the read-out process, the information just read out must be delivered after a suitable delay to write amplifier 99 for rewriting in order to preserve the memory content, unless new information is to be written in. This is accomplished by the above device 90. For the sake of clarity, Fig. 3 shows only one arrangement of sense amplifier 79, write amplifier 99, and device 90.

The following describes the mode of operation of the magnetic film memory. The word pulse initiating the read-out process passed from pulse source 57 *via* a branch of the conductor to the two transistors 55 and 56 of the first level of the twitch pyramid. Which is these two transistors is activated is determined by the address register 58, which by means of conductors 64 and 65 controls the first level of the switch pyramid. The transistor 55 of the first level is activated when a suitable potential is applied, e.g. *via* control conductor 64. In this example let it be assumed further that a corresponding activating potential for transistors 51 to 54 of the second level is applied by means of address register 58 *via* control conductor 66. Transistors 52 and 54 are thus activated. The word pulse delivered by pulse source 57 and passed on *via* transistor 55 in the first level reaches the two transistors 51 and 52 of the second level through a branch of the conductor; only the latter transistor is activated, so that the pulse ultimately reaches word line 31. In the figure the pulse propagating toward the short-circuited end of the selected word line 21 is shown. In this process the magnetization vectors of the magnetic film memory cells arranged adjacent to word line 21 are switched to the hard direction. The switching of magnetization induces in the

associated sense lines 71 to 78 sense pulses that are to be read out in parallel in accordance with the binary information stored.

It is a disadvantage of known magnetic film memories that the read-out process involves the destruction of the information stored in the magnetic film memory cell. A new word pulse is therefore required for rewriting the information in a subsequent writing or regeneration cycle. In the present invention the generation of a separate rewrite pulse by source 57 can be eliminated, since the pulse passing through delay means such as the conductor extension 86 is reflected by the short-circuit, and returns with reversed polarity into the same word line, e.g. 21, with a suitable delay. This is schematically shown in Fig. 3 by the other pulse adjacent to word line 21. In this process the magnetization vectors of the magnetic film memory cells are again switched to the hard direction. Thus for example the writing process required for regeneration can be undertaken without a second pulse having to be delivered by pulse source 57. For the writing of new information into the magnetic film memory cells of a selected word, the computer delivers the appropriate signals, representing individual binary values, simultaneously and in parallel to the associated input terminal, such as terminal 98*a*, of write amplifiers 99. In the case of regeneration of the information just read out, appropriate signals pass from sense amplifiers 79 *via* devices 90 to write amplifiers 99 with a suitable delay. A simple logical circuit at the input of the write amplifiers determines whether the writing cycle is to consist of regeneration or the writing is of new information.

After regeneration or writing in, the returning pulse must generally be attenuated, preferably in such a manner that the initial word pulse passing to the right is not also attenuated. In the second embodiment according to Fig. 3 such an asymmetric attenuation arrangement is shown on each word line 11, 21, 31, 41 by shunt means comprising a diode 84 and a resistance 85. In many cases, suitable attenuation can be achieved by the switching means *per se* which are in any case required for word line selection. For example, in the embodiment of Fig. 1, the function of the attenuation arrangement is taken over by diodes 12*a* to 45*a* in conjunction with distribution busses 16 to 46, or by the transmission losses.

WHAT WE CLAIM IS:—

1. A binary information store, including a matrix of columns and rows of storage elements each of magnetic material exhibiting uniaxial anisotropy; a plurality of word lines each common to a column of storage elements and each connected at one end through a gate to a connection with an input line which extends between the respective connection and a source of high frequency pulses each having a steep front, in which store each input line and/or each word line is or are extended on the side of the respective line connection remote from the pulse source so that any pulse reflected from the ends of the extensions arrives back at each line connection delayed by more than a chosen amount relatively to the time of arrival of the original pulse at the respective line connection.

2. A binary information store, including a matrix of magnetic storage elements each exhibiting uniaxial magnetic anisotropy; a plurality of groups of word lines, the word lines of each group being connected through gates to connections with one of a plurality of input lines which extend between the connections and a plurality of sources of high frequency pulses each having a steep front, in which store either or both of the input and word lines are extended on the sides of the line connections remote from the pulse source so that any pulses reflected from the ends of the extensions arrive back at the connections delayed by more than a chosen amount relatively to the time of arrival of the orignal pulses at the line connections.

3. A store as claimed in claim 1 or 2, in which the or each input line is extended intermediate its line connections and its pulse source, whereby a pulse reflected from the line connections and again reflected by the pulse source is delayed in arrival back at the line connections by more than a chosen amount relatively to the time of arrival of the original pulse at the line connections.

4. A store as claimed in any preceding claim, in which each line has a resistor at its end, on the side of the respective line connection remote from the pulse source, and in which the resistance of the or each resistor is smaller than the resistive component of the characteristic impedance of the line in which it is inserted.

5. A store as claimed in claim 4, in which the resistance of the resistor is greater than 0.42 times the resistive component of the characteristic impedance.

6. A store as claimed in claim 5, in which the resistance of the or each resistor is 0.7 times the resistive component of the characteristic impedance.

7. A store as claimed in any preceding claim, in which each storage element is a film of uniaxial anisotropic magnetic material.

8. A store as claimed in claim 7, in which pulses reflected from the ends of the word lines remote from the input lines are used to switch the direction of magnetisation of the thin film elements associated with the word line to the hard direction for subsequent regeneration cycles.

9. A store as claimed in claim 8, in which each row of storage elements has associated

with it a pair of read and write lines provided with a circuit arrangement including a logical circuit combined with a delay device, which circuit is capable of feeding back the information read out from the read-line amplifier into the input of an amplifier in the write line for the regeneration of the contents of the store just read out.

10. A store as claimed in claim 8 or 9, in which each word line is provided with an assymetrical attenuator which does not affect the initial pulses but which attenuates reflected pulses.

11. A store as claimed in claim 10, in which each assymetrical attenuator consists of a diode connected in series with a resistor, the diode being poled to block the initial pulses but to pass the reflected pulses.

12. A magnetic information store substantially as described herein with reference to Figures 1 and 2 of the accompanying drawings.

13. A store substantially as described herein with reference to Figure 3 of the accompanying drawings.

14. A method of operating a store as claimed in claims 12 or 13, substantially as described herein.

For the Applicants,
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Chartered Patent Agent.

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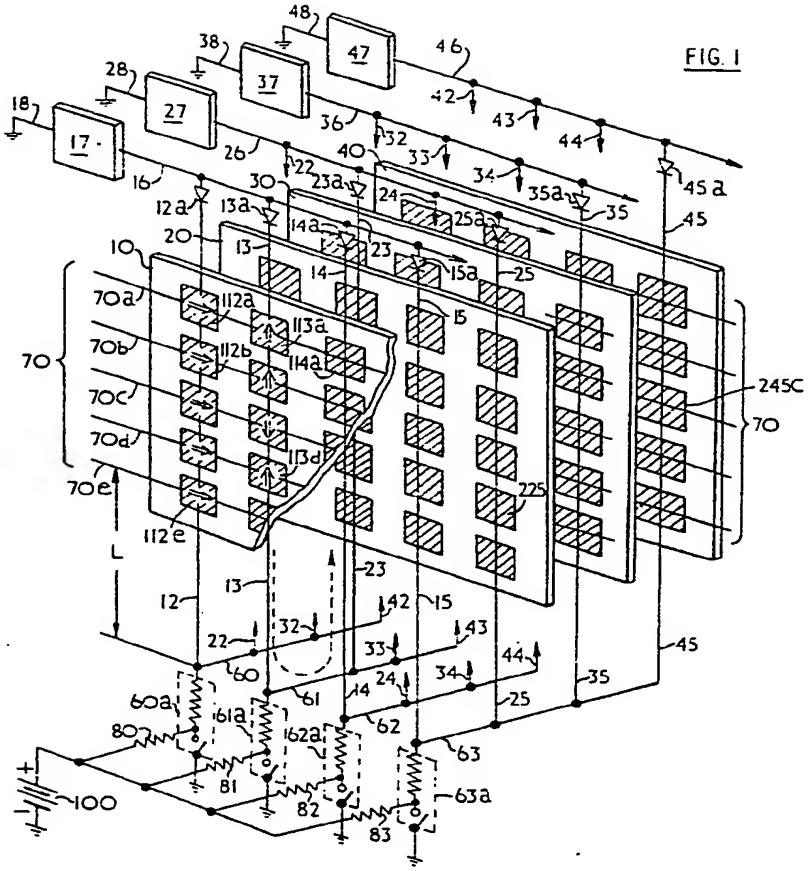


FIG. 1

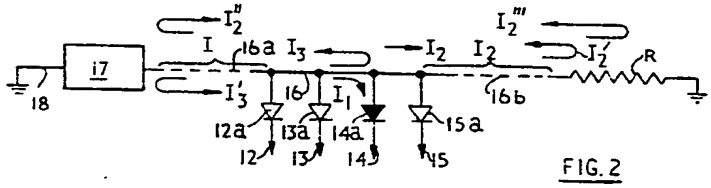
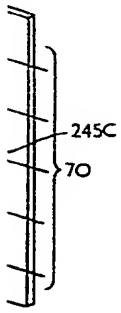


FIG. 2

1003489 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 1 & 2

IG. 1



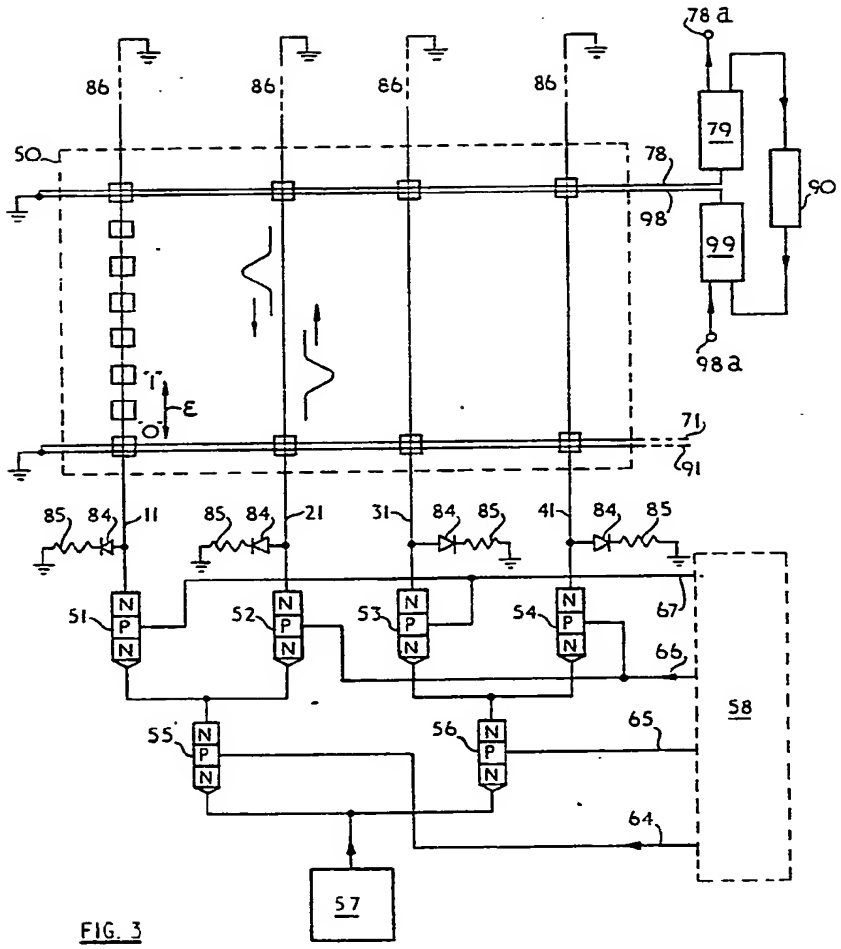


FIG. 3

1003489 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 1 & 2

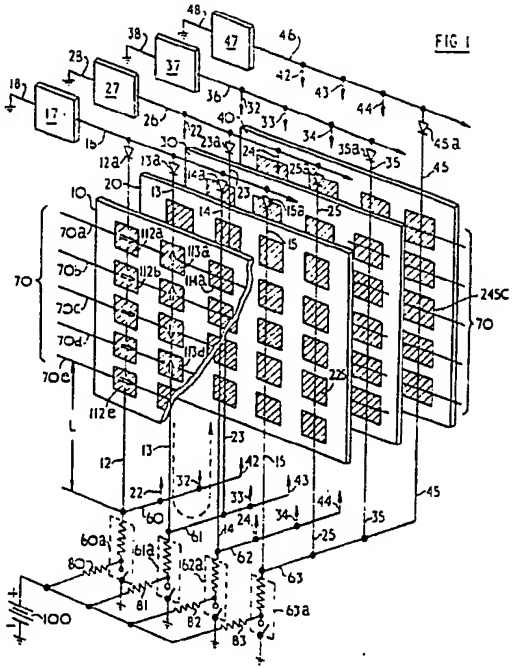


FIG 1

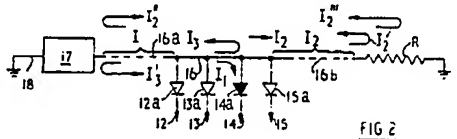


FIG 2

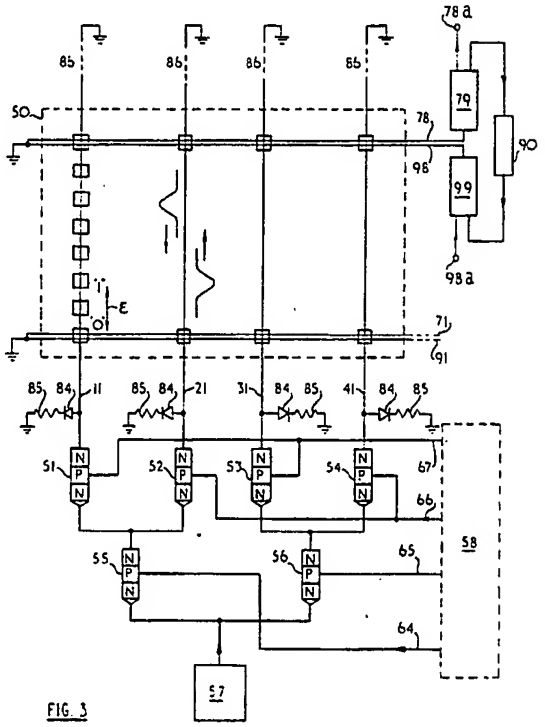


FIG 3